MSB1218A-RT1

Preferred Device

PNP Silicon General Purpose Amplifier Transistor

This PNP Silicon Epitaxial Planar Transistor is designed for general purpose amplifier applications. This device is housed in the SC−70/SOT−323 package which is designed for low power surface mount applications.

Features

- High h_{FE}, 210−460
- Low $V_{CE(sat)}$, < 0.5 V
- Pb−Free Package is Available

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Collector−Base Voltage	$V_{(BR)CBO}$	45	Vdc
Collector−Emitter Voltage	$V_{(BR)CEO}$	45	Vdc
Emitter−Base Voltage	$V_{(BR)EBO}$	7.0	Vdc
Collector Current − Continuous	I_C	100	mAdc
Collector Current − Peak	$I_{C(P)}$	200	mAdc

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Power Dissipation (Note 1)	P_D	150	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Collector−Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	45	−	Vdc
Collector−Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	45	−	Vdc
Emitter−Base Breakdown Voltage (I_E = 10 μAdc, I_E = 0)	$V_{(BR)EBO}$	7.0	−	Vdc
Collector−Base Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	−	0.1	μA
Collector−Emitter Cutoff Current (V_{CE} = 10 Vdc, I_B = 0)	I_{CEO}	−	100	μA
DC Current Gain (Note 2) (V_{CE} = 10 Vdc, I_C = 2.0 mAdc)	h_{FE1}	210	340	−
Collector−Emitter Saturation Voltage (Note 2) (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	−	0.5	Vdc

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Device mounted on a FR−4 glass epoxy printed circuit board using the minimum recommended footprint.
2. Pulse Test: Pulse Width ≤ 300 μs, D.C. ≤ 2%.

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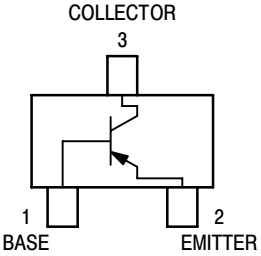
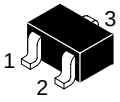
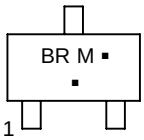




SC−70 (SOT−323)
CASE 419
STYLE 4

MARKING DIAGRAM



BR = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MSB1218A−RT1	SC−70	3000 /Tape & Reel
MSB1218A−RT1G	SC−70 (Pb−Free)	3000 /Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

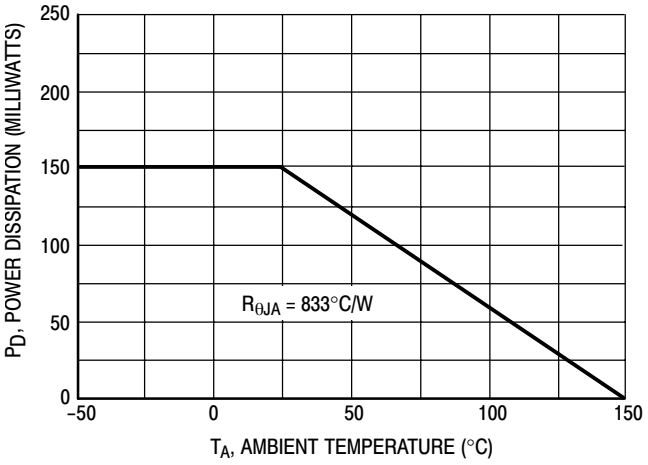


Figure 1. Derating Curve

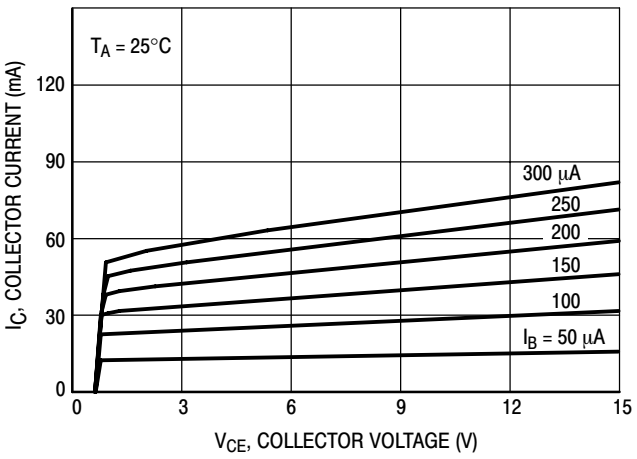


Figure 2. $I_C - V_{CE}$

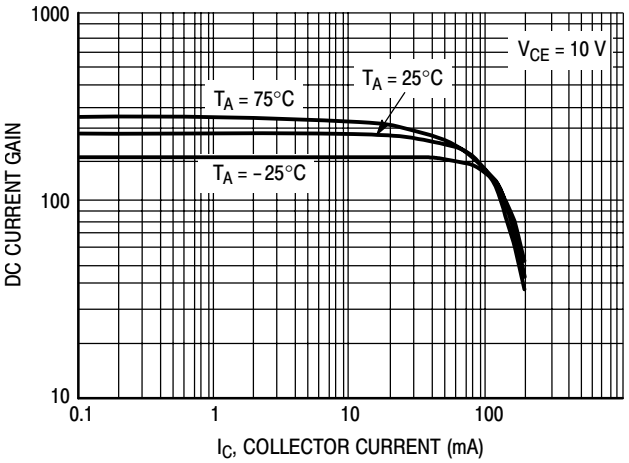


Figure 3. DC Current Gain

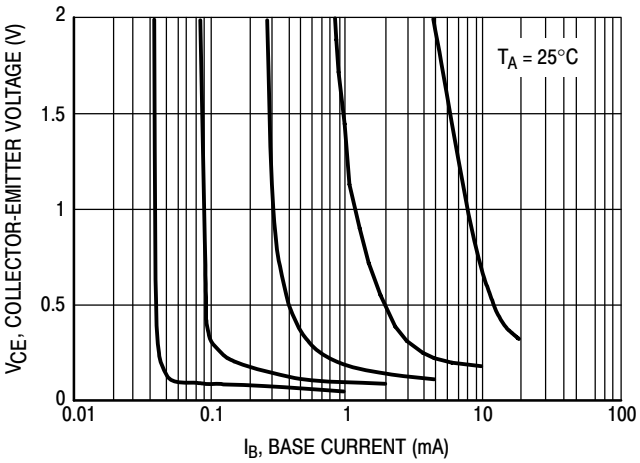


Figure 4. Collector Saturation Region

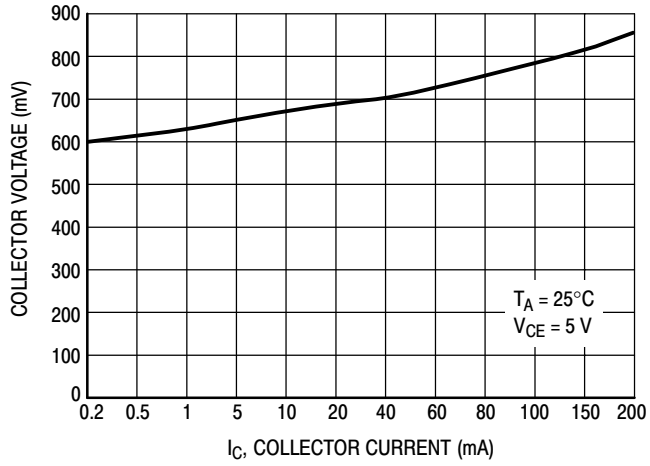


Figure 5. On Voltage

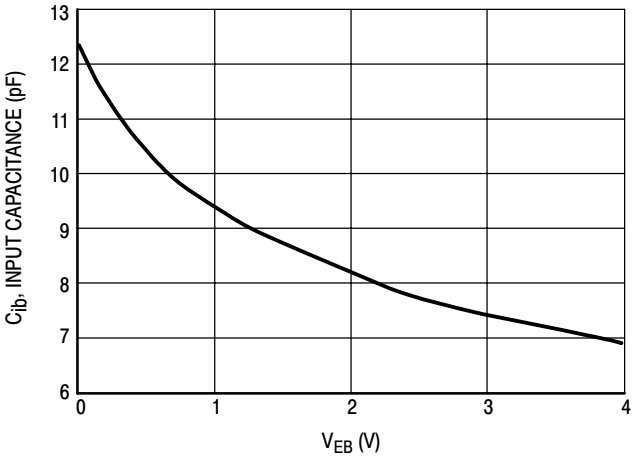


Figure 6. Capacitance

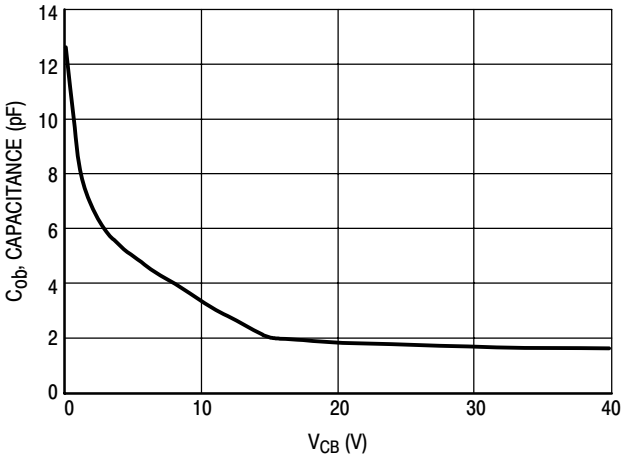
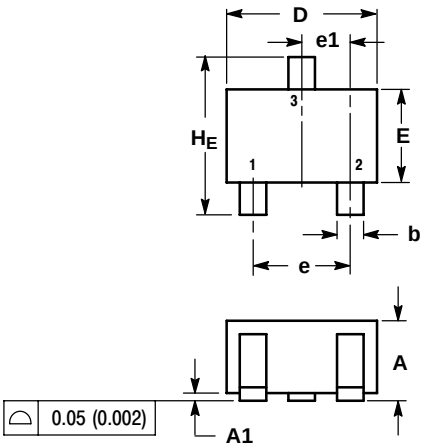


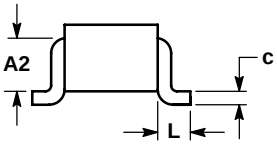
Figure 7. Capacitance

MSB1218A−RT1

PACKAGE DIMENSIONS

SC−70 (SOT−323)
CASE 419−04
ISSUE M



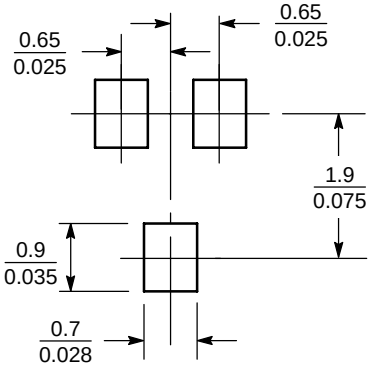


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.7 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L		0.425 REF			0.017 REF	
H_E	2.00	2.10	2.40	0.079	0.083	0.095

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
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